ΑΝΑΡΤΗΤΕΑ ΣΤΟ ΔΙΑΔΙΚΤΥΟ

ΕΛΛΗΝΙΚΗ ΔΗΜΟΚΡΑΤΙΑ

ΥΠΟΥΡΓΕΙΟ ΑΝΑΠΤΥΞΗΣ ΚΑΙ ΕΠΕΝΔΥΣΕΩΝ

ΓΕΝΙΚΗ ΓΡΑΜΜΑΤΕΙΑ ΕΡΕΥΝΑΣ ΚΑΙ ΚΑΙΝΟΤΟΜΙΑΣ

ΙΔΡΥΜΑ ΤΕΧΝΟΛΟΓΙΑΣ ΚΑΙ ΕΡΕΥΝΑΣ

ΙΝΣΤΙΤΟΥΤΟ ΠΛΗΡΟΦΟΡΙΚΗΣ

Ταχ. Διεύθυνση: Ν. Πλαστήρα 100

70013 Ηράκλειο Κρήτης

Αρ.Πρωτ. 68748

Ηράκλειο 22/12/2021

Call for expression of interest for one (1) position of Experienced RTL Design and Test Engineer, in the Institute of Computer Science (ICS) Foundation for Research and Technology – Hellas (FORTH)

Position(s): One (1) position for the eProcessor project

Project: eProcessor (GA 956702) funded under H2020-JTI-EuroHPC-2019-1.

Duration: 5 months with possibility of extension
Location: Heraklion, Crete, Greece
Opening date: 22/12/2021
Closing date: 07/01/2022
Reference: "Project_eProcessor_Experienced RTL Design and Test_Dec2021"

Description

We seek one (1) Experienced RTL Design and Test Engineer for our team. The candidate should have proven multi-year experience on hardware RTL design, integration and validation with a background in European Research Projects. The candidate will participate in the R&D activities of FORTH in the context of the EuroHPC JU project eProcessor. The eProcessor project combines open source software (SW)/hardware (HW) to deliver the first completely open source European full stack ecosystem based on a new RISC-V CPU coupled to multiple diverse accelerators that target traditional HPC and extend into mixed precision workloads for High Performance Data Analytics (HPDA), (AI, ML, DL and Bioinformatics). eProcessor will be extendable (open source), energy-efficient (low power), extreme-scale (high performance), suitable for uses in HPC and embedded applications, and extensible (easy to add on-chip and/or off-chip components).

Requirements:

- University degree from School of Sciences or Engineering.
- At least 10 years of documented professional experience in related roles.
- At least 10 years of experience in European Research Projects.
- Demonstrated experience in Verilog and SystemVerilog RTL design and system development projects.

- Demonstrated experience in FPGA systems development and Xilinx Vivado Design Suite.
- Demonstrated experience with on-chip interconnects and communication protocols such as: AMBA5 CHI, AXI, and PCIe.
- Demonstrated experience with Memory Management Units (MMU), DMA engines, high-speed network interfaces and RDMA for large scale systems.
- Physical presence at FORTH, Heraklion, Crete for the duration of the position.
- Fluent knowledge of English.
- Names of at least three professional references.

Desired qualifications:

- Experience with test-driven development and validation.

Application Submission

Interested candidates can submit their applications via http://www.ics.forth.gr/jobs using the link "Apply for the position" under the announcement. Applications must include:

- Detailed CV, including qualifications and interests in the above areas, and proof thereof
- Scanned copies of academic and other titles

Promising candidates may be invited for an interview before a decision is made.

Contact Information

- For information and questions regarding the application and selection procedure, please contact: webmaster@ics.forth.gr
- For information and questions about the advertised positions, the activities of the group, or the Institute, please contact Nikolaos Papadopoulos (nickpap@ics.forth.gr)

Selection Announcement

The result of the selection will be announced on the website of ICS-FORTH. Candidates have the right to appeal the selection decision, by addressing their written objection to the ICS secretariat within five (5) days since the results announcement on the web. They also have the right to access (a) the files of the candidates as well as (b) the table of candidates' scores (ranking of candidates results). All the above information related to the selection procedure will be available at the secretariat of ICS-FORTH in line with the Hellenic Data Protection Authority. Access to personal data of co-candidates shall be limited to personal data (and relevant data) and supporting documents which have been the basis of the evaluation of the candidates for the specific post(s). Prior to the announcement of the personal data and/or documents of the co-candidates to the applicant, FORTH will inform the data subjects in an appropriate way.

FORTH is compliant with all legal procedures for the processing of personal data as defined by the **Regulation EU/2016/679 on the protection of natural persons with regard to the processing of personal data.**

FORTH processes the personal data and relevant supporting documents that you have submitted to us. Processing of that data is carried out exclusively for the needs and purposes of this specific call. Such data shall not be transmitted to or communicated to any third party unless required by law.

FORTH retains the above data up to the announcement of the final results of the call, unless further process and reservation is required by law or for purposes of exercise, enforcement, prosecution of certain one's legitimate legal rights' as defined in the Regulation EU/2016/679 and/or in national law.

We inform you that under the **Regulation EU/2016/679** you have the rights to be informed about your personal data, access to, rectification and erasure, restrictions of process and objection to as provided by applicable regulation and national laws.

We acknowledge also to you, that you have the right to file a complaint to the national Data Protection Authority. For any further information regarding exercise of your personal data protection rights, you may contact the Data Protection Officer at FORTH at dpo@admin.forth.gr.

You have the right to withdraw your application and consent for the processing of your personal data at any time. We inform you that, in this case, FORTH shall destroy such documents and/or supporting documents submitted and shall delete the related personal data.